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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/978,528	10/17/2001	Andres Bryant	BU9-99-055	5054

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EXAMINER	
SEFER, AHMED N	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/978,528	BRYANT ET AL.	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25,27-31,34 and 35* is/are pending in the application.

4a) Of the above claim(s) *1-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-25,27-31,34 and 35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/21/2004 has been entered. Claims 32-33 have been cancelled and new claims 34-35 have been introduced.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: Reference numeral 17 mentioned in the specification (see page 7, lines 2 and 18-20) is not shown in figs. 6 and 7. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

DETAILED ACTION

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 23-25 and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Deleonibus ("Deleonibus") USPN 6,091,076 in view of Koh ("Koh") USPN 6,049,110.

Deleonibus discloses in figs. 1 and 2 a semiconductor device comprising a semiconductor layer formed on an insulating layer 44; a gate conductor 20 formed on the semiconductor layer; spacers 24/26 formed on sidewalls of the gate conductor and on the semiconductor layer; extension regions 8, 10 extending further under the spacers than diffusion regions 4, 6 (as in claim 28) arranged in the semiconductor layer on both sides of the gate conductor and extending at least under the spacers, wherein a portion of at least one of the extensions regions is exposed at a surface of the semiconductor layer; diffusion regions 4, 6 formed in the semiconductor layer adjacent to the extension regions; and a metal layer 12/14 contacting the diffusion region (as in claim 25) formed at least in the exposed portion of the extension region, the metal layer contacting the semiconductor layer and the exposed portion of the extension region, but does not disclose extension regions extending and contacting said spacer and a portion of said gate conductor.

Koh discloses in fig. 43 a semiconductor device comprising a semiconductor layer formed on an insulating layer 31 including extension regions (regions under reference numerals

55 and 56) extending further under the spacers 55 arranged in the semiconductor layer on both sides of a gate conductor 56 and extending under and contacting the spacers and a portion of the gate conductor.

Since Koh and Deleonibus are both from the same field of endeavor, MOS transistors, the teaching disclosed by Koh would have been recognized in the pertinent art of Deleonibus. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Koh's teachings with Deleonibus' device since that would suppress short channel effects as taught by Koh.

As to claim 24, Deleonibus discloses extension regions lower doped than the diffusion regions.

As to claim 27, Deleonibus discloses extension region exposed on both sides of the gate conductor at the surface of the semiconductor layer and the metal layer formed in both the exposed portions of the extension regions.

As to claim 29, Deleonibus discloses the metal layer and the exposed portion of the extension region form an schottky diode.

As for removing at least a part of one of the spacers or at least a portion of each spacer recited in claims 23 and 27 respectively, it refers to a portion(s) which is not part of a final structure implying a process and product by process" claims are directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685 and In re Thorpe, 227 USPQ 964, 966. Therefore, the way the product was made does not carry any patentable weight as long as the claims are directed to a device. Further, note

that the applicant has the burden of proof in such cases, as the above case law makes clear. Also see MPEP 2113.

5. Claims 23-25 and 27-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al. ("Yamaguchi") USPN 5,341,028 in view of Imai ("Imai") USPN 6,297,529 and Koh.

Yamaguchi discloses in figs. 5 and 6 a semiconductor device comprising a semiconductor layer formed on an insulating layer 12; a gate conductor 20 formed on the semiconductor layer; spacers 25/26 formed on sidewalls of the gate conductor and on the semiconductor layer; extension regions 15, 16 extending further under the spacers than diffusion regions 17, 18 (as in claim 28) arranged in the semiconductor layer on both sides of the gate conductor and extending at least under the spacers, wherein a portion of at least one of the extensions regions is exposed at a surface of the semiconductor layer; diffusion regions 17, 18 formed in the semiconductor layer adjacent to the extension regions; a metal layer 27 contacting the diffusion region (as in claim 25) formed at least in the exposed portion of the extension region, but do not disclose said extension regions extending and contacting said spacer and a portion of said gate conductor or said metal layer contacting the semiconductor layer the exposed portion of the extension region.

Imai discloses in fig. 2 a semiconductor device comprising a semiconductor layer 5/6; a gate conductor 14; extension regions 16 extending further under spacers 17 than diffusion regions 19 arranged in the semiconductor layer on both sides of the gate conductor and extending at least under the spacers; and a metal layer 20 formed at least in the exposed portion of the extension region and extending into the semiconductor layer (as in claim 30) or extends into a

portion of the semiconductor layer below said extension region (as in claim 31), the metal layer contacting the semiconductor layer the exposed portion of the extension region.

Koh discloses in fig. 43 a semiconductor device comprising a semiconductor layer formed on an insulating layer 31 including extension regions (regions under reference numerals 55 and 56) extending further under the spacers 55 arranged in the semiconductor layer on both sides of a gate conductor 56 and extending under and contacting the spacers and a portion of the gate conductor.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Imai's teachings with Yamaguchi's device since that would prevent an increase of the contact resistance of the gate electrode with the metal layer. It would have been obvious to incorporate Koh's teachings since that would suppress short channel effects as taught by Koh.

As to claim 24, Yamaguchi discloses extension regions lower doped than the diffusion regions.

As to claim 27, Yamaguchi discloses extension region exposed on both sides of the gate conductor at the surface of the semiconductor layer and the metal layer formed in both the exposed portions of the extension regions.

As to claim 29, Yamaguchi discloses the metal layer and the exposed portion of the extension region form an schottky diode.

As for removing at least a part of one of the spacers or at least a portion of each spacer recited in claims 23 and 27 respectively, it refers to a portion(s) which is not part of a final structure implying a process and product by process" claims are directed to the product per se, no

matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685 and In re Thorpe, 227 USPQ 964, 966. Therefore, the way the product was made does not carry any patentable weight as long as the claims are directed to a device. Further, note that the applicant has the burden of proof in such cases, as the above case law makes clear. Also see MPEP 2113.

6. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi in view of Gardner et al. ("Gardner") USPN 6,096,615 and Koh.

Yamaguchi discloses in figs. 5 and 6 an integrated circuit disposed on an SOI substrate having a body region 14, comprising a transistor having a source diffusion region 17, a gate formed over said body region, a first sidewall spacer disposed on a side wall of said gate abutting the source diffusion region, a drain diffusion region 18, a second sidewall spacer disposed on a side wall of said gate abutting the drain diffusion region, and extension regions extending further under the gate than the source and the drain diffusion regions, wherein a portion of at least one of the extension regions is exposed at a surface of the body region; and a conductor 27 formed at least in the exposed portion of the extension region, the conductor being in contact with the exposed portion of the extension region and at least a portion of the source diffusion region to form a Schottky diode, but do not disclose extension regions provided under and contacting first and second sidewall spacers, the extension regions contacting said gate and extending further under the gate or a first sidewall spacer thinner than a second sidewall spacer.

Gardner discloses (see fig. 2G and col. 5, lines 1-15) an integrated circuit comprising a first sidewall spacer 210 thinner than a second sidewall spacer 219.

Koh discloses in fig. 43 a semiconductor device comprising a semiconductor layer formed on an insulating layer 31 including extension diffusion regions (regions under reference numerals 55 and 56) provided under and contacting first and second sidewall spacers 55, said extension diffusion regions contacting said gate and extending further under the gate conductor 56 and extending further under said gate conductor.

Since Yamaguchi, Koh and Gardner are all from the same field of endeavor, MOS transistors, the teachings disclosed by Koh and Gardner would have been recognized in the pertinent art of Yamaguchi. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Gardner's teachings since that would be useful in subsequent dopant implant step as taught by Gardner. It would have been obvious to incorporate Koh's teachings since that would suppress short channel effects as taught by Koh.

As for removing at least a part of one of the first and a second sidewall sapcers recited in the claim, it refers to a portion(s) which is not part of a final structure implying a process and product by process" claims are directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685 and In re Thorpe, 227 USPQ 964, 966. Therefore, the way the product was made does not carry any patentable weight as long as the claims are directed to a device. Further, note that the applicant has the burden of proof in such cases, as the above case law makes clear. Also see MPEP 2113.

7. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi in view of Gardner and Koh as applied to claim 32 above, and further in view of Imai.

The combined references disclose the device structure as recited in the claim, but fail to disclose a conductor in contact with a body region.

Imai discloses in fig. 2 an integrated circuit having a body region 5/6; a gate conductor 14; extension regions 16 extending further under spacers 17 than diffusion regions 19 arranged in the semiconductor layer on both sides of the gate conductor and extending at least under the spacers; and a conductor 20 contacting the body region.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Imai's teachings since that would prevent an increase of the contact resistance of the gate electrode with the conductor layer.

8. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Deleonibus in view of Gardner and Koh.

Deleonibus discloses in fig. 2 an integrated circuit disposed on an SOI substrate having a body region 42, comprising a transistor having a source diffusion region 4, a gate 20 formed over said body region, a first sidewall spacer 20 disposed on a side wall of said gate abutting the source diffusion region, a drain diffusion region 6, a second sidewall spacer 26 disposed on a side wall of said gate abutting the drain diffusion region, and extension regions extending further under the gate than the source and the drain diffusion regions, wherein a portion of at least one of the extension regions is exposed at a surface of the body region; and a conductor 12/14 formed at least in the exposed portion of the extension region, the conductor being in contact with the exposed portion of the extension region and at least a portion of the source diffusion region to form a Schottky diode, but do not disclose extension regions provided under and contacting first and second sidewall spacers, the extension regions contacting said gate and extending further under the gate or a first sidewall spacer thinner than a second sidewall spacer.

Gardner discloses (see fig. 2G and col. 5, lines 1-15) an integrated circuit comprising a first sidewall spacer 210 thinner than a second sidewall spacer 219.

Koh discloses in fig. 43 a semiconductor device comprising a semiconductor layer formed on an insulating layer 31 including extension regions (regions under reference numerals 55 and 56) extending further under the spacers 55 arranged in the semiconductor layer on both sides of a gate conductor 56 and extending under and contacting the spacers and a portion of the gate conductor.

Since Deleonibus, Koh and Gardner are all from the same field of endeavor, MOS transistors, the teachings disclosed by Koh and Gardner would have been recognized in the pertinent art of Deleonibus. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Gardner's teachings since that would be useful in subsequent dopant implant step as taught by Gardner. It would have been obvious to incorporate Koh's teachings since that would suppress short channel effects as taught by Koh.

As for removing at least a part of one of the first and a second sidewall sapcers recited in the claim, it refers to a portion(s) which is not part of a final structure implying a process and product by process" claims are directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685 and In re Thorpe, 227 USPQ 964, 966. Therefore, the way the product was made does not carry any patentable weight as long as the claims are directed to a device. Further, note that the applicant has the burden of proof in such cases, as the above case law makes clear. Also see MPEP 2113.

9. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Deleonibus in view of Gardner and Koh as applied to claim 32 above, and further in view of Imai.

The combined references disclose the device structure as recited in the claim, but fail to disclose a conductor in contact with a body region.

Imai discloses in fig. 2 an integrated circuit having a body region 5/6; a gate conductor 14; extension regions 16 extending further under spacers 17 than diffusion regions 19 arranged in the semiconductor layer on both sides of the gate conductor and extending at least under the spacers; and a conductor 20 contacting the body region.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Imai's teachings since that would prevent an increase of the contact resistance of the gate electrode with the conductor layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANS
November 24, 2004